

REMARKS

This paper responds to the Office Action mailed on July 30, 2007.

Claims 13 and 58 are amended. Claims 13-16, 48-65, and 76-78 remain pending in this application.

Applicant maintains all arguments presented in all previous amendment and responses and submits additional arguments below.

§112 Rejection of the Claims

Claims 13-16 were rejected under 35 U.S.C. § 112, second paragraph, for indefiniteness.

Applicant respectfully traverses. Claim 13 is amended to replace “the first supply node” with “the first and second supply nodes”. Therefore, Applicant requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 112, second paragraph.

§103 Rejection of the Claims

Claims 13-16, 48-65, and 76-78 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Namekawa (U.S. 6,115,301).

Applicant respectfully traverses for at least the reasons presented below.

Independent claim 13

Claim 13, as amended, recites in part, that the corresponding internal node is coupled to the first storage node of each of the memory cells through only one first transistor, and the corresponding internal node is coupled to the second storage node of each of the memory cells through only one second transistor. The Office Action, page 7, compares memory segments in element 10 of FIG. 1 of Namekawa to the memory segments of claim 13. But, the Office Action does not specifically point out which elements of Namekawa are being compared to the internal nodes of claim 13. Regarding the internal nodes in general, the Office Action, page 7, points to a passage in column 3, lines 23-25 of Namekawa. However, in this passage, Namekawa does not specifically teach an internal node that is coupled to a first storage node of each of the memory cells of memory segments in element 10 of FIG. 1 of Namekawa. Namekawa also does not specifically teach an internal node that is coupled to a second storage node of each of the

memory cells of memory segments in element 10 of FIG. 1 of Namekawa. In contrast, claim 13 recites that the corresponding internal node is coupled to the first storage node of each of the memory cells through only one first transistor, and the corresponding internal node is coupled to the second storage node of each of the memory cells through only one second transistor.

Claim 13, as amended, also recites in part, that each of the memory cells is electrically disconnected from the corresponding internal node when the corresponding memory segment is electrically disconnected from the corresponding internal node. The Office Action, page 7, compares element 70 in FIG. 1 of Namekawa to the switching units of claim 48. However, as described in column 6 lines 5-30 of Namekawa, element 70 in FIG. 1 of Namekawa includes decoder circuits, such as D1 and D15, to control switch circuit groups 50 and 60 to replace a defective data line with a redundant data line. Applicant submits that element 70, or switch circuit group 50, or 60 in FIG. 1 of Namekawa are not function in ways such that each of the memory cells in element 10 of FIG. 10 of Namekawa is electrically disconnected from a corresponding internal node when a corresponding memory segment in element 10 of FIG. 10 of Namekawa is electrically disconnected from the corresponding internal node.

The reasons presented above demonstrate that claim 13 is patentable over Namekawa because Namekawa does not teach every element recited in claim 13. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claim 13.

Dependent claims 14-16 and 76

Dependent claims 14-16 and 76 depend from claim 13. Thus, Applicant believes that claims 14-16 and 76 are also patentable over Namekawa for at least the reasons presented above regarding claim 13, plus the additional things recited in claims 14-16 and 76.

Independent claim 58

Claim 58, as amended, recites in part, that the internal node is coupled to the first storage node of each of the memory cells through only one first transistor, and the internal node is coupled to the second storage node of each of the memory cells through only one second transistor. For the reasons at least similar to those presented above regarding claim 1, Applicant submits that Namekawa does not teach an internal node that is coupled to the first storage node

of each of the memory cells through only one first transistor, and the internal node is coupled to the second storage node of each of the memory cells through only one second transistor.

Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claim 58.

Dependent claims 59-62 and 77

Dependent claims 59-62 and 77 depend from claim 58. Thus, Applicant believes that claims 59-62 and 77 are also patentable over Namekawa for at least the reasons presented above regarding claim 58, plus the additional things recited in claims 59-62 and 77. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claims 59-62 and 77.

Independent claim 48

Claim 48 recites, in part, a first supply node to provide a first supply source and a second supply node to provide a second supply source. The Office Action does not specifically point out which element of Namekawa is being compared to the first supply node of claim 48 to provide the first supply. The Office Action also does not specifically point out which element of Namekawa is being compared to the second supply node of claim 48 to provide the second supply source. To reject this part of claim 48, the Office Action, page 8, points to a passage in column 7, lines 3-20 of Namekawa. But the Office Action does not point out where in this passage a person can find a first supply node to provide a first supply source and a second supply node to provide a second supply source. Since the Office Action does not specifically point out which elements of Namekawa are being compared to the first and second supply node of claim 48, Applicant assumes that the Office Action compares Vcc, as described in column 7, lines 3-20 of Namekawa, to the first supply node of claim 48 and the ground, as described in column 7, lines 3-20 of Namekawa, to the second supply node of claim 48.

Claim 48 also recites, in part, a first internal node to receive the first supply source from the first supply node. The Office Action does not point out, and Applicant is unable to find, where in Namekawa a person can find a teaching of an internal node that is arranged and

connected to other elements in such ways that are recited in claim 48 to receive a first supply source from a first supply node.

Claim 48 also recites, in part, a second internal node to receive the second supply source from the second supply node. The Office Action does not point out, and Applicant is unable to find, where in Namekawa a person can find a teaching of an internal node that is arranged and connected to other elements in such ways that are recited in claim 48 to receive a first supply source from a first supply node.

Claim 48 also recites, in part, a plurality of memory segments, each of the memory segments including a plurality of memory cells. The Office Action, page 8, explicitly compares memory segments and memory cells in element 10 of FIG. 1 of Namekawa to the memory segments and the memory cells of claim 48. Thus, in this amendment and response, Applicant follows the comparison by Office Action and considers that the memory segments in element 10 of FIG. 1 of Namekawa are being compared to the memory segments of claim 48, and that the memory cells in element 10 of FIG. 1 of Namekawa are being compared to the memory cells of claim 48.

Claim 48 also recites, in part, that each of the memory cells includes a first storage node and a second storage node. The Office Action, page 8, points to element 80 in FIG. 2 of Namekawa and asserts that each of the memory cells include a first storage node and a second storage node. Applicant respectfully traverses because the Office Action here uses another element (element 80) to compare it with the memory cells of claim 48, instead of using the same memory cells in element 10 of FIG. 1 of Namekawa (as discussed immediately above). Even if element 80 in FIG. 2 of Namekawa is used to compare to memory cells of claim 48, element 80 in FIG. 2 of Namekawa includes fuse circuits, decoders, and transfer gates. In contrast, claim 48 recites memory cells. Nevertheless, even if the Office Action consider the same memory cells in element 10 of FIG. 1 of Namekawa, each of the memory cells in element 10 of FIG. 1 has *only* one storage node, which is the node between transistor TR and a capacitor CC. In contrast, claim 48 recites two storage nodes: a first storage node and a second storage node.

Claim 48 also recites, in part, that each of the memory cells includes a latch connected to the first and second storage nodes and connected in between the first internal node and the second internal node. The Office Action does not specifically points out which element of

Namekawa is being compared to the latch of claim 48 in which the latch is connected to the first and second storage nodes and connected in between the first internal node and the second internal node. To reject this part of claim 48, the Office Action, page 8 and continuing to page 9, points to a passage in column 1 lines 5-40 of Namekawa. But the Office Action does not point out where in this passage a person can find a latch and its connections to other elements such ways that are recited in claim 48. In reviewing the passage in column 1 lines 5-40 of Namekawa, applicant submits that Namekawa teaches some general parts of a dynamic random access memory (DRAM) device and that Namekawa does not teach a latch and its connections such ways that are recited in claim 48. In contrast, claim 48 recites that each of the memory cells includes a latch connected to the first and second storage nodes and connected in between the first internal node and the second internal node.

Claim 48 also recites, in part, that each of the memory cells includes a first access element for accessing the first storage node and a second access element for accessing the second storage node. The Office Action does not specifically point out which element of Namekawa is being compared to the first access element of claim 48 for accessing the first storage node. The Office Action also does not specifically point out which element of Namekawa is being compared to the second access element of claim 48 for accessing the second storage node. To reject this part of claim 48, the Office Action points to a passage in column 6 lines 25-50 of Namekawa to reject this part of claim 48. But the Office Action does not point out where in this passage a person can find first and second access elements and their function to access the first and second storage nodes of the memory cell of Namekawa. In reviewing the passage in column 6 lines 25-50 of Namekawa, Applicant submits that Namekawa teaches functions of element 80 and the functions of other elements of FIG. 1 of Namekawa such as switches SW10, SW 24, SW24, and decoders D0 and D15. Applicant submits that Namekawa does not teach the elements and their functions such as the access elements and their functions of claim 48. As discussed above, the Office Action compares memory cells in element 10 of FIG. 1 of Namekawa to the memory cells of claim 48. Here, regarding the passage in column 6 lines 25-50 of Namekawa that the Office Action uses to reject the part related to the access elements of claim 48, Applicant is unable to find in this passage a teaching that each of the memory cells includes first and second access elements for accessing first and second storage nodes of the

memory cells memory cells in element 10 of FIG. 1 of Namekawa. In contrast, claim 48 recites that each of the memory cells includes a first access element for accessing the first storage node and a second access element for accessing the second storage node.

Claim 48 also recites, in part, a plurality of first switching units, each of the first switching units connecting in between the first supply node and a corresponding memory segment of the memory to prevent the corresponding memory segment from receiving the supply source from the first internal node connected to the corresponding memory segment when the corresponding memory segment has a defect. The Office Action does not specifically points out which elements of Namekawa are being compared to the first switching units connecting in between the first supply node and a corresponding memory segment of the memory to prevent the corresponding memory segment from receiving the supply source from the first internal node connected to the corresponding memory segment when the corresponding memory segment has a defect. To reject this part of claim 48, the Office Action, page 9, points to a passage in column 3 lines 23-50 of Namekawa. But the Office Action does not point out where in this passage a person can find of the first switching units and their functions as recited in claim 48. In reviewing passage in column 3 lines 23-50 of Namekawa, applicant submits that Namekawa teaches a first switch group having a plurality of switches connecting to data lines. Applicant submits that Namekawa does not teach plurality of switches and their connection in ways and functions as those of the first switching units claim 48. As discussed above, the Office Action compares memory segments in element 10 of FIG. 1 of Namekawa to the memory cells of claim 48. Here, regarding the passage in column 3 lines 23-50 of Namekawa that the Office Action uses to reject the part related to the first switching units of claim 48, Applicant is unable to find in this passage a teaching that the first switch group of Namekawa are being connected in between the first supply node and a corresponding memory segment in element 10 of FIG. 1 of Namekawa, and that this first switch group can somehow prevent the corresponding memory segment in element 10 of FIG. 1 of Namekawa from receiving the supply source from a first internal node connected to the corresponding memory segment when the corresponding memory segment has a defect. In contrast, claim 48 recites a plurality of first switching units, each of the first switching units connecting in between the first supply node and a corresponding memory segment of the memory to prevent the corresponding memory segment from receiving the supply

source from the first internal node connected to the corresponding memory segment when the corresponding memory segment has a defect.

Claim 48 also recites, in part, a plurality of second switching units, each of the second switching units connecting between the second supply node and a corresponding memory segment of the memory segments to prevent the corresponding memory segment from receiving a supply source from the second internal node connected to the corresponding memory segment when the corresponding memory segment is defective. To reject this part of claim 48, the Office Action, page 9, compares element 70 in FIG. 1 of Namekawa to the plurality of second switching units of claim 48 and also points to passage in column 6 lines 5-30 of Namekawa. Applicant respectfully traverses. As described in column 6 lines 5-30 of Namekawa, element 70 in FIG. 1 of Namekawa includes decoder circuits, such as D1 and D15, to control switch circuit groups 50 and 60 to replace a defective data line with a redundant data line. Applicant submits that element 70, or switch circuit group 50, or 60 in FIG. 1 of Namekawa and their connections and functions are different from those of the second switching units of claim 48. As discussed above, the Office Action compares memory segments in element 10 of FIG. 1 of Namekawa to the memory cells of claim 48. Here, regarding element 70 of the passage in column 6 lines 5-30 of Namekawa that the Office Action uses to reject the part related to the second switching units of claim 48, Applicant is unable to find in this passage a teaching that element 70, or switch circuit group 50, or 60 in FIG. 1 of Namekawa are being connected in between the second supply node and a corresponding memory segment in element 10 of FIG. 1 of Namekawa, and that 70, or switch circuit group 50, or 60 in FIG. 1 of Namekawa can somehow prevent the corresponding memory segment in element 10 of FIG. 1 of Namekawa from receiving the supply source from a second internal node connected to the corresponding memory segment when the corresponding memory segment has a defect. In contrast, claim 48 recites a plurality of second switching units, each of the second switching units connecting between the second supply node and a corresponding memory segment of the memory segments to prevent the corresponding memory segment from receiving a supply source from the second internal node connected to the corresponding memory segment when the corresponding memory segment is defective.

The reasons presented above demonstrate that claim 48 is patentable over Namekawa because Namekawa does not teach every element recited in claim 48. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claim 48.

Dependent claims 49-57

Dependent claims 49-57 depend from claim 48. Thus, Applicant believes that claims 49-57 are also patentable over Namekawa for at least the reasons presented above regarding claim 48, plus the additional things recited in claims 49-57.

For example, claim 50 recites that at least one of the memory segments has a circuit short between the first and second internal nodes. The Office Action points to a passage in column 4, lines 3-50 of Namekawa to support the rejection of claim 50. However, this passage only teaches, in part, control of the switches that are located between defective data line and a redundant data line. Applicant submits that this passage does not teach at least one of the memory segments, such as one of the memory segments in element 10 of FIG. 1 of Namekawa, has a circuit short between the first and second internal nodes. In contrast, claim 50 recites that at least one of the memory segments has a circuit short between the first and second internal nodes.

In another example, claim 53 recites that each of the first switching units includes a transistor having a source and a drain connected between the first supply node and one of the memory segments. The Office Action points to a passage in column 5, lines 37-50 of Namekawa to support the rejection of claim 53. However, this passage teaches elements 10 and 20, which include DRAM cells. Applicant submits that this passage does not teach first switching units in which each of the first switching units includes a transistor having a source and a drain connected between the first supply node and one of the memory segments. In contrast, claim 53 recites that each of the first switching units includes a transistor having a source and a drain connected between the first supply node and one of the memory segments.

In another example, claim 54 recites that each of the second switching units includes a transistor having a source and a drain connected between the second supply node and one of the memory segments. As in the case of claim 53, the Office Action points to the passage in column 5, lines 37-50 of Namekawa to support the rejection of claim 54. However, as discussed above regarding claim 53, this passage teaches elements 10 and 20 including DRAM cells. Applicant

submits that this passage does not teach second switching units in which each of the second switching units includes a transistor having a source and a drain connected between the first supply node and one of the memory segments. In contrast, claim 53 recites that each of the second switching units includes a transistor having a source and a drain connected between the second supply node and one of the memory segments.

In another example, claim 48 recites that each of the memory cells include a latch, and claim 55 further recites that the latch includes a first inverter having an input node connected to the first storage node and an output node connected to the second storage node, and a second inverter having an input node connected to the second storage node and an output node connected to the first storage node. The Office Action points to the passage in column 8, lines 25-40 of Namekawa to support the rejection of claim 55. However, this passage teaches more details of the device of FIG. 1 of Namekawa including details of the decoder circuits with NAND gates and inverters. Applicant submits that this passage does not teach a latch of a memory cell, such as the memory cell of memory segment in element 10 of FIG. 1 of Namekawa. As discussed above regarding claim 48, the Office Action compares memory cells in element 10 of FIG. 1 of Namekawa to the memory cells of claim 48. Here, regarding the passage in column 8, lines 25-40 of Namekawa that the Office Action uses to reject claim 55, Applicant is unable to find in this passage a teaching of a latch of a memory cell in element 10 of Namekawa in which the latch includes a first inverter having an input node connected to the first storage node and an output node connected to the second storage node, and a second inverter having an input node connected to the second storage node and an output node connected to the first storage node. In contrast, claim 53 recites that the latch includes a first inverter having an input node connected to the first storage node and an output node connected to the second storage node, and a second inverter having an input node connected to the second storage node and an output node connected to the first storage node.

In another example, claim 48 recites that each of the memory cells include first and second access elements, and claim 56 further recites that one of the first and second access elements includes a transistor having a source and a drain connected between one of the first and second storage nodes and a bit line. The Office Action points to the passage in column 5, lines 37-50 of Namekawa to support the rejection of claim 56. However, as discussed above

regarding claims 53 and 54, this passage teaches elements 10 and 20 including DRAM cells. Applicant submits that this passage does not teach that each of the memory cells include first and second access elements in which one of the first and second access elements includes a transistor having a source and a drain connected between one of the first and second storage nodes and a bit line. In contrast, claim 56 recites that one of the first and second access elements includes a transistor having a source and a drain connected between one of the first and second storage nodes and a bit line.

In another example, claim 48 recites that each of the memory cells include a latch, and claim 57 recites that the latch includes a first pair of transistors having a common drain connected to the first storage node and a common gate connected to the second storage node, and a second pair of transistors having a common drain connected to the second storage node and a common gate connected to the first storage node. The Office Action to the passage in column 5, lines 37-50 of Namekawa to support the rejection of claim 57. However, as discussed above regarding claims 53, 54, and 56, this passage teaches elements 10 and 20 including DRAM cells. Applicant submits that this passage does not teach a latch including a first pair of transistors having a common drain connected to the first storage node and a common gate connected to the second storage node, and a second pair of transistors having a common drain connected to the second storage node and a common gate connected to the first storage node. In contrast, claim 57 recites that the latch includes a first pair of transistors having a common drain connected to the first storage node and a common gate connected to the second storage node, and a second pair of transistors having a common drain connected to the second storage node and a common gate connected to the first storage node.

The reasons presented above demonstrate that claims 49-57 are patentable over Namekawa because Namekawa does not teach every element recited in claims 49-57. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claims 49-57.

Independent claim 63

Claim 63 recites, in part, isolating a selected memory segment of the memory segments from the corresponding internal node connected to the selected memory segment if the selected

memory segment is defective to prevent the selected memory segment from receiving the supply source at the corresponding internal node connected to the selected memory segment. The Office Action does not offer a specific reason why claim 63 is rejected. The Office Action only states that since Namekawa teaches a device as discussed above regarding claims 13-16 and 48-57, Namekawa also teaches the method claimed by claim 63. Applicant respectfully disagrees. Applicant submits that Namekawa teaches a device that is different from the one claimed in claim 13-16 and 48-57, as discussed in details above regarding claims 13-16 and 48-57. For example, the device in FIG. 1 of Namekawa teaches a method of replacing a defective data line with a redundant data line. Applicant submits that the method of Namekawa, while it teaches replacing a defective data line with a redundant data line, does not teach isolating a selected memory segment in element 10 of FIG. 1 of Namekawa from the corresponding internal node connected to the selected memory segment if the selected memory segment in element 10 of FIG. 1 is defective to prevent the selected memory segment from receiving the supply source at the corresponding internal node connected to the selected memory segment. In contrast, claim 63 recites isolating a selected memory segment of the memory segments from the corresponding internal node connected to the selected memory segment if the selected memory segment is defective to prevent the selected memory segment from receiving the supply source at the corresponding internal node connected to the selected memory segment.

Dependent claim 64-65 and 78

Dependent claims 64-65 and 78 depend from claim 63. Thus, Applicant believes that claims 64-65 and 78 are also patentable over Namekawa for at least the reasons presented above regarding claim 63, plus the additional things recited in claims 64-65 and 78.

For example, claim 65 recites isolating the memory segment includes electrically disconnecting the memory segment from the supply source. As described above regarding claim 63, Namekawa teaches a method of replacing a defective data line with a redundant data line. Applicant submits that the method of Namekawa, while it teaches replacing a defective data line with a redundant data line, does not teach electrically disconnecting the selected memory segment in element 10 of FIG. 1 of Namekawa from the corresponding internal node connected to the selected memory segment. In contrast, claim 65 recites electrically disconnecting the

selected memory segment from the corresponding internal node connected to the selected memory segment.

The reasons presented above demonstrate that claims 64-65 and 78 are patentable over Namekawa because Namekawa does not teach every element recited in claims 64-65 and 78. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claims 64-65 and 78.

RESERVATION OF RIGHTS

In the interest of clarity and brevity, Applicant may not have addressed every assertion made in the Office Action. Applicant's silence regarding any such assertion does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's representative at (612) 373-6969 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 30th day of October 2007.

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